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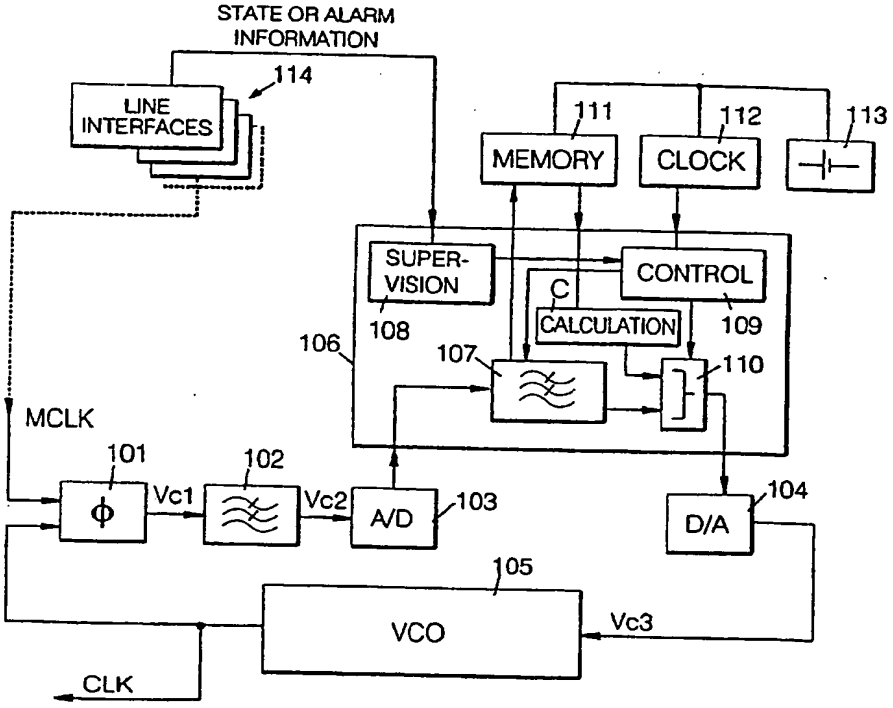
(54) Title: METHOD OF GENERATING A CLOCK SIGNAL BY MEANS OF A PHASE-LOCKED LOOP AND A PHASE-LOCKED LOOP

(57) Abstract

The invention relates to a method of generating a clock signal (CLK) by means of a phase-locked loop, and a phase-locked loop comprising a phase comparator (101), a loop filter (102), and a voltage-controlled oscillator (105). In the method, a synchronizing signal (MCLK) derived from a synchronisation source is applied to first input in the phase comparator (101), and the clock signal is locked to the synchronizing signal. In order that the clock frequency could be kept unchanged even in failure situations, a control voltage sequence of the oscillator (105) is stored in a memory (111) over a predetermined period of time while the clock signal is locked to the synchronizing signal, and a sequence obtained from the memory is substituted for the control voltage obtained from the phase comparator (101) in response to a change where a currently applied synchronizing signal becomes inadequate for use in timing.



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# Method of generating a clock signal by means of a phase-locked loop and a phase-locked loop

The invention relates to a method according to the preamble of the attached claim 1 for generating a clock signal by means of a phase-locked loop, and to a phase-locked loop according to the preamble of the attached claim 7. The method and the phase-locked loop according to the invention can be applied primarily in slave oscillators of digital telecommunication systems, i.e. oscillators intended to be locked to the master clock signal of the system.

In present-day digital transmission systems, synchronization can be performed by the use of either separate synchronizing connections or normal data connections between system nodes (devices). Separate synchronizing connections are used only in individual cases and very seldom for the synchronization of the entire network. When data connections are used for synchronization, the line code should be such that even the clock frequency can be extracted from an incoming data signal by the nodes. These clock frequencies allow the synchronization of network nodes to be performed by two different basic methods: mutual synchronization and master-slave synchronization. In mutual synchronization each node derives its own clock frequency from the average value of the frequencies of incoming signals and its own current clock frequency. In this way, all nodes in the network are driven towards a common average frequency, and achieve it in stable state. However, a network utilizing mutual synchronization cannot be synchronized with a desired source, so that it is problematic to interconnect e.g. different networks, as the operating frequency of the entire network cannot thereby be accurately determined

in advance. In master-slave synchronization, instead, all network nodes are synchronized with the clock frequency of a specific node called a master node. Each node selects the frequency of a single incoming signal as the source of its own clock frequency. The node tends to select a signal having the clock frequency of the master node of the network.

In independent master-slave synchronization, each node makes the synchronization decision independently without any external information supporting the decision making. As the nodes make their synchronization decision independently, each node has to contain specifications defining the node with which this node should be synchronized. These specifications are often in the form of a priority list, and the node selects the signal of the highest priority from amongst incoming signals of adequate quality as its source of synchronization. If the signal breaks or its quality deteriorates so that it is no longer adequate for use as a source of synchronization, the node selects the signal having the next highest priority from the list. The priority list has to be selected so that all nodes contained in it are located between the concerned node and the master mode, so that the synchronization will be distributed from the master node to the lower levels.

Independent master-slave synchronization, however, imposes limitations on synchronization: in a loop network all connections cannot be used for synchronization, whereby the dynamic adaptability of the network in different situations is limited. Internodal communication has to be established to ensure that each individual node has enough information for decision making in all situations without having to drastically limit the number of connections available

for synchronization, whereby the clock frequency of the master node could not be equally efficiently distributed to the network nodes in failure situations.

Loop protected (LP) synchronization is the simplest method of making independent master-slave synchronization more communicative. LP synchronization aims to prevent the losing of timing in loop networks by using, in addition to the above-mentioned priority lists, two state bits mcb and lcb transmitted between network nodes. The first state bit mcb (master control bit) indicates whether the network synchronization originates from the master node of the network. The master node defined for the network transmits this bit as a logic zero in its outgoing signals, and other nodes forward it if they are synchronized with a signal in which the value of the mcb bit is zero. The second state bit lcb (loop control bit) indicates whether a loop is formed in synchronization. Each network node transmits this bit as a logic one in the direction in which it is synchronized itself, and as a logic zero in all other directions.

Each node uses its own priority list on selecting its source of synchronization, but it checks not only the state of the signal but also the mcb and lcb bits before making the selection. In the first place, the node aims to find a connection having a clock frequency originating from the master node of the network (mcb=0). If such a connection cannot be found (due to a failure situation), the node selects, as normal, an operative connection having the highest priority. However, it is always required from the selected connection (the source of timing) that its timing is not in a loop (lcb=0), even though the signal itself would otherwise be of adequate quality

for synchronization.

In order that the heavy specifications of the LP synchronization (which usually still have to be changed when nodes are added to or removed from the network) could be avoided, internodal communication should be extended from two state bits to messages. In this kind of message-based master-slave synchronization the node is able to make the decision concerning its own synchronization on the basis of synchronizing messages contained in incoming signals. No priority list is thereby needed, and all network connections can be used for synchronization. The synchronizing message contains all synchronization information required by the node. The node has to know the origin of the synchronization of the signal containing the synchronizing message in order that it would be synchronized with a clock frequency originating from the master node of the network. The messages also have to contain sufficiently other information in order that the node could select the best one from available alternatives, and in order that synchronization loops would not be formed. One prior art message-based synchronization method is the SOMS (Self-Organizing Master-Slave Synchronization) method, which is described more fully e.g. in Finnish Patent Applications 925 070 - 925 074. Message-based synchronization methods are also described in US Patents 2,986,723 and 4,837,850.

The method and phase-locked loop according to the present invention are intended for use in telecommunication networks utilizing synchronization methods of the type described above, where a network node has to synchronize with a master clock signal.

A problem with these networks is that differences are created between the clock frequencies of

different devices (nodes) of the network in connection with changes in the synchronization source. Such changes may be e.g. a failure of the master clock source or a break in connections between some network portions. When the network portions operate at different clock frequencies, bit error bursts occur between them. The number of bursts is the higher the greater the difference between the clock frequencies.

Traditionally the oscillators of digital transmission systems have been switched to free oscillation in the absence of an incoming master clock. At the production stage, free oscillation is attempted to be adjusted to the nominal centre frequency. This method, however, does not usually provide good results, as

- the properties of the oscillator may have varied with time,
- the adjustment of the centre frequency is not usually made with any particularly high accuracy,
- the master clock frequency may differ from the nominal frequency,
- upon transition of the oscillator from the state of free oscillation to the locked state, or *vice versa*, there may occur drastic instantaneous frequency changes,
- the effect of temperature and environmental conditions cannot be taken into account, and
- jitter occurring in the master clock cannot be taken into account.

Improvements have been made in phase-locked loops to dispense with the above-mentioned drawbacks. One improvement is reading the voltage controlling the oscillator into a memory through an analog-to-digital converter during normal operation. When the locking source is then lost, the control voltage is derived from the memory by a digital-to-analog converter

during the break. This method has e.g. the following drawbacks:

- the output voltage of the digital-to-analog converter is not steplessly adjustable,
- the effect of temperature and other environmental conditions cannot be taken into account, and
- jitter occurring in the master clock cannot be taken into account.

The object of the present invention is to dispense with the above drawbacks and to provide a method by means of which differences between clock frequencies used in different portions of a digital transmission network can be kept as small as possible during time periods when synchronization between the different network portions is lost. This is achieved by a method and phase-locked loop according to the invention. The method is characterized by what is disclosed in the characterizing portion of the attached claim 1, while the phase-locked loop is characterized by what is disclosed in the characterizing portion of the attached claim 7.

The solution according to the invention allows the clock frequency to be kept substantially unchanged when the synchronization of the network is lost.

In the following the invention will be described more fully by way of example while referring to Figure 1 of the attached drawings, which is a block diagram illustrating the structure of a phase-locked loop used in the method according to the invention.

The phase-locked loop shown in Figure 1 comprises, as is known *per se*, a phase comparator 101, a lowpass-type loop filter 102 having an input to which an output signal from the phase comparator is connected, and a voltage-controlled oscillator 105 having its output signal connected to one comparator input in

the phase comparator. A master clock signal MCLK originating from the synchronization source (the master node of the network) and obtained from line interface circuits 114 is connected to another comparator input in the phase comparator. The phase comparator compares the phases of the signals present in its inputs and generates a control signal Vc1 proportional to the phase difference between the signals. The control signal is lowpass-filtered in the loop filter 102 into a control signal Vc2. The clock signal CLK of the device (node) is obtained from the output of the voltage-controlled oscillator 105, and, as is well-known, the phase-locked loop tends to control the output signal of the oscillator such that there is no phase difference between the signals present in the comparator inputs of the phase comparator; in other words, the output signal of the oscillator is locked to the frequency of the master clock signal.

According to the invention a digital filter block 106 implemented by a processor is integrated in the phase-locked loop on one hand by providing an analog-to-digital converter 103 after the loop filter 102, the output signal of the converter being fed to the filter block, and on the other hand by connecting the output signal of the filter block through a digital-to-analog converter 104 to the input of the voltage-controlled oscillator 105 as the voltage Vc3 controlling the frequency of the oscillator.

The filter or processor block 106 comprises a digital lowpass filter 107 having an input to which the output signal of the analog-to-digital converter 103 is connected and subjecting the control voltage Vc2, already lowpass filtered once, to additional filtration. The block further comprises a supervision

unit 108, a control unit 109 controlled by the supervision unit, and a selector 110 controlled by the control unit 109. The filter block further has an associated separate control voltage memory 111, which stores the variation sequence of the control voltage obtained from the filter 107 over a predetermined period of time.

The output signal of the digital lowpass filter 107 is connected to one input in the selector, and the output signal of the memory 111 is connected to another input in the selector either directly or through a separate calculation unit C. The output of the selector is connected to the digital-to-analog converter 104.

In practice, the entire filter block 106 may be implemented by an effective telecommunication processor, whereby the supervision and control units can be implemented entirely by software. The processor may be e.g. of the type 68HC302 or another general-purpose processor of the same level. Instead, it is not advisable to implement the filter block 106 by a signal processor, as the filtration load is light in typical operation. (At present, it is regarded that e.g. a solution where the bandwidth of the prefilter 102 is about 100 Hz, the bandwidth is decreased to 10 Hz, and a slope no greater than 20 dB/decade is needed, is fairly good. A prefilter of greater bandwidth or a greater slope would increase the processor power required for filtration.)

The filter block further has an associated real-time clock 112, which indicates time to the control unit 109 and which is secured by a battery 113 in case of a break in the supply of electricity. The continuously updated memory 111 is preferably a non-volatile memory, the operation of which is secured by the same

battery. The real-time clock is needed especially in storing a long-term control voltage sequence (which will be described below).

Furthermore, state and alarm information is connected from the line interface circuits 114 of the device (node) to the input of the supervision unit 108.

It is further to be noted that the phase-locked loop typically comprises (between the oscillator and the phase comparator) a divider, which, however, is not shown in the figure, as it is not relevant to the present invention.

The phase-locked loop according to the invention operates in the following way.

In a normal situation when the clock signal CLK is locked to a master clock signal MCLK originating from the synchronization source (the master node of the network), the control signal Vc1 from the phase comparator 101 is lowpass-filtered in the loop filter 102. The filtered control signal Vc2 is applied through the analog-to-digital converter 103 to the digital lowpass filter 107, from which it is connected, after further filtration, through the digital-to-analog converter 104 as the voltage Vc3 controlling the frequency of the oscillator 105. In this situation, the control unit 109 has thus controlled the selector 110 into a position in which the input, to which the output signal of the digital lowpass filter 107 is connected, is connected to the output of the selector. Detection of locking is based on state and alarm information received in the supervision unit from the line interface circuits 114, which may include e.g. the following:

- an alarm indication that an adequate signal is present in the input interface from which the timing

(master clock signal) is to be derived;

- the state of the LP timing bits is such that it is not necessary to change the timing source; or

- the state of the SOMS timing message is such that it is not necessary to change the timing source.

In this normal state a variation sequence of the control voltage obtained from the digital lowpass filter 107 is stored continuously in the memory 111 under the control of the control unit 109. The length of the sequence stored in the memory at a specific time depends on the use. If it can be assumed that the master oscillator of the network is of high quality especially with respect to long-term stability (temperature compensated, etc.), and what is needed is merely to improve the tolerance of short-term inaccuracies, such as errors caused by jitter, the storage of a few samples over a short period (e.g. a few minutes) is enough. On the contrary, if it is also regarded as necessary to compensate for frequency changes occurring over a longer period of time, such as changes caused by temperature variations at different times of the day, the storage should be made over the desired period. Typically, twenty-four hours is a suitable period. The sampling period is limited mainly by the memory space reserved for the purpose; on the other hand, it cannot be assumed that there would occur deviations of more than ± 50 ppm from the centre frequency in a properly built, operative digital transmission system, if there are no timing errors; and if the network is to remain e.g. "SDH synchronous" (± 4.6 ppm), it can be assumed that e.g. 512 samples (about 20 samples per hour) would be enough.

When the supervision unit 108 receives from the line interface circuits 114 of the device (node) an

indication that there is no longer a master clock signal adequate for use as a locking source, the filter block 106 (processor) substitutes a sequence obtained from the memory for the control voltage from the phase comparator. Detection of the need for substitution is based on state or alarm information from the line interface circuits, which may include e.g. the following information:

- an alarm indication that a signal is missing from the input interface of the device (node) from which the timing (master clock signal) has been derived, or an alarm indication that the signal of the input interface has deteriorated to such an extent that it can no longer be used for synchronization;
- a change in the state of the LP timing bits such that it is necessary to change the timing source; or
- a change in the state of the SOMS timing message such that it is necessary to change the timing source.

If the storage of samples has been performed over a short period of time, a few of the last samples have to be rejected as they cannot be regarded as reliable due to system delays. In other words, it is necessary to reject samples if it is not known for sure upon the detection of failure that they originate from the master clock. The rest of the samples are averaged, and the average obtained is connected through the selector 110 and the digital-to-analog converter 104 to control the oscillator 105. Calculation is represented by a separate unit C in the figure. On the contrary, if the storage of samples has been performed over a long period of time, the real-time clock 112 indicates the right storing times and the right starting point for the sequence. This se-

quence is connected (under the control of the control unit) through the selector 110 and the digital-to-analog converter 104 to control the oscillator 105. The form of the control voltage formed by the sequence can be improved by calculating intermediate values between the stored samples in the calculation unit C.

One suitable edge point for a sequence having the length of twenty-four hours is midnight. It is preferable to store two sequences at a time in the memory, i.e. a sequence to be used and a sequence to be edited, which are changed at a time corresponding to the edge point of the sequence. (Information indicating which one of the sequences is to be used also has to be stored in a non-volatile manner).

After a signal adequate for timing is again found, the normal situation described above is resumed, whereby the control voltage of the oscillator is obtained from the phase comparator.

Even though the invention has been described above with reference to the examples of the attached drawings, it is self-evident that the invention is not limited to them, but it can be modified within the inventive idea disclosed above and in the attached claims. For instance, the details of the implementation of the filter block realized by a processor for performing the same functions may vary. The solution according to the invention is not either necessarily limited to the generation of the clock signal of a node in a digital telecommunication network, but other applications of the same type are possible as well.

Claims:

1. Method of generating a clock signal (CLK) by means of a phase-locked loop comprising a phase comparator (101), a loop filter (102), and a voltage-controlled oscillator (105), wherein a synchronizing signal (MCLK) derived from a synchronization source is applied to a first input in the phase comparator (101), and the clock signal is locked to the synchronizing signal, characterized in that a control voltage sequence of the oscillator (105) is stored in a memory (111) over a predetermined period of time while the clock signal is locked to the synchronizing signal, and the sequence obtained from the memory is substituted for the control voltage obtained from the phase comparator (101) in response to a change where a currently applied synchronizing signal becomes inadequate for use in timing.

2. Method according to claim 1, characterized in that the voltage values of the sequence stored in the memory are averaged, and the obtained average is substituted for the control voltage obtained from the phase comparator.

3. Method according to claim 1, characterized in that the waveform of the sequence obtained from the memory is improved by calculating intermediate values between the stored values.

4. Method according to claim 1, characterized in that the control voltage sequence is stored substantially over a period of twenty-four hours.

5. Method according to claim 4, characterized in that two sequences at a time are stored in the memory, that is, a sequence available for the substitution of the control voltage and a

sequence to be edited.

6. Method according to claim 4, c h a r a c t e r i z e d in that 20 to 25 samples are taken per hour.

7. Phase-locked loop for generating a clock signal, comprising a phase comparator (101), a loop filter (102), and a voltage-controlled oscillator (105), a synchronizing signal (MCLK) from a synchronization source being connected to an input in the phase comparator (101), and the clock signal being locked to the synchronizing signal, c h a r a c t e r i z e d in that it comprises means (107, 111, 112) for storing a control voltage sequence of the oscillator (105) over a predetermined period of time while the clock signal is locked to the synchronizing signal, and means (108-110, 112) for substituting said sequence for the control signal obtained from the phase comparator (101) in response to a change where a currently applied synchronizing signal becomes inadequate for use in timing.

8. Phase-locked loop according to claim 7, c h a r a c t e r i z e d in that said storing means comprise a digital lowpass filter (107) and a non-volatile memory (111) in which samples from said lowpass filter are stored, and that said substituting means comprise a selector (110) to the inputs of which signals obtained from the digital lowpass filter (107) and the memory (111) are connected.

9. Phase-locked loop according to claim 7, c h a r a c t e r i z e d in that said storing and substituting means comprise a real-time clock (112) for indicating the right storing time and the right starting point for the sequence.

10. Phase-locked loop according to claim 7, c h a r a c t e r i z e d in that it further com-

prises a calculation unit (C) for calculating intermediate values between values stored in the memory (111).

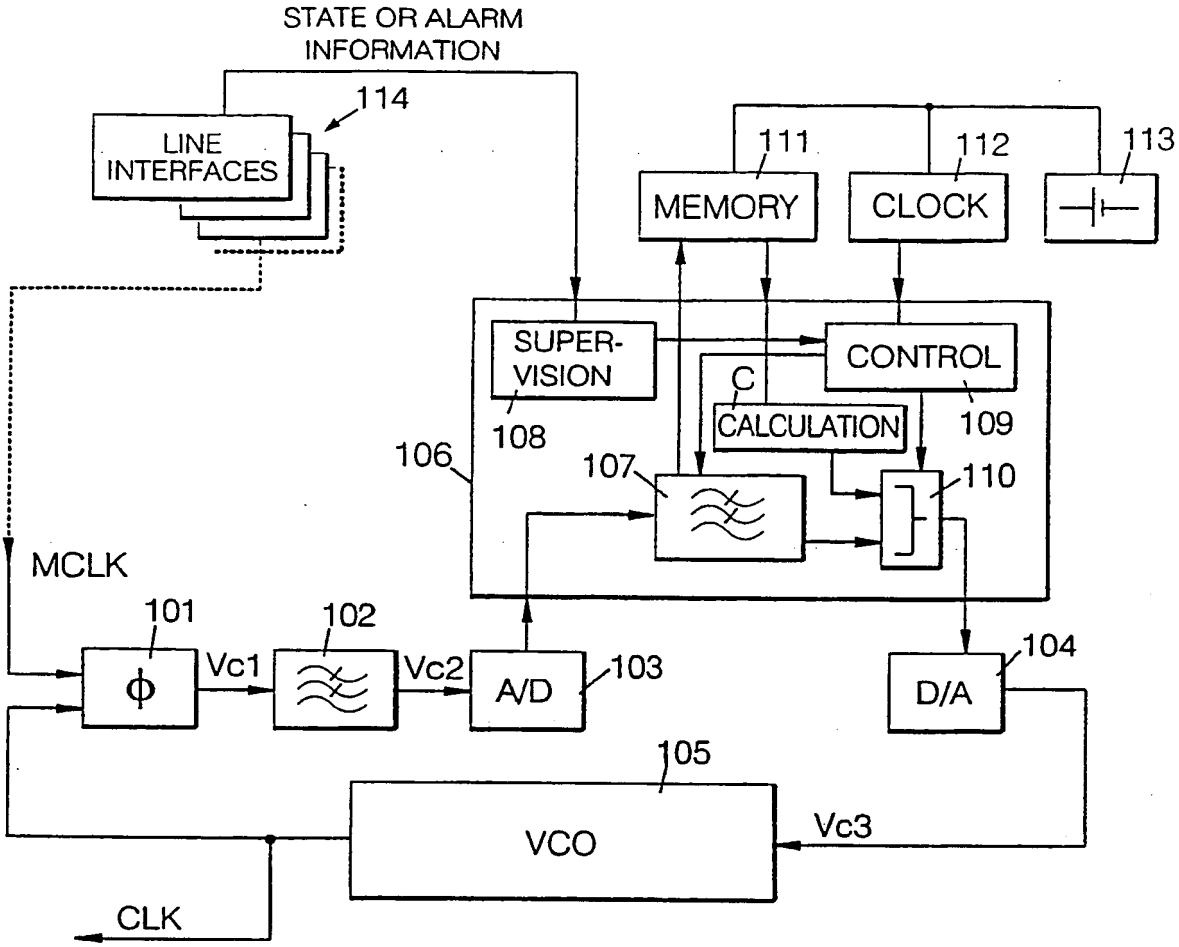


FIG. 1

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A. CLASSIFICATION OF SUBJECT MATTER

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B. FIELDS SEARCHED

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IPC 5: H03L, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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Information on patent family members

28/05/94

International application No.
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